**Senior Physical Design Engineer**

**Designation:**

**Senior Physical Design Engineer**

**Experience Level:**

**6+ years of hands-on physical design experience**

**Responsibilities:**

* **Responsibilities will include block level and sub system ownership of designs, unit level verification and complete design reviews for signoff.**
* **Own the activities from RTL to GDS and sign off of few blocks and sub systems.**
* **Mentor the junior team members for physical design convergence.**
* **Work with multiple sites in a team environment.**

**Requirements:**

* **Bachelors/Masters in ECE from a reputed University.**
* **Candidate is expected to work on RTL to GDS flows for complex designs with processor cores and IPs.**
* **Good hands on experience with Million gates with multiple power domains and multiple clocks.**
* **Good Hands on experience of working with Multi modes, multi RC corners and multiple PVT corners.**
* **To be responsible for and own all aspects of physical design and physical verification efforts at block level and subsystem levels.**
* **Good knowledge of EDA tools from Synopsys, Cadence and Mentor required.**
* **Good Experience with tools like ICC, INNOVUS, PTSI, First Encounter, Nanoroute, Calibre, StarRC, and Conformal is essential.**
* **Good knowledge of VLSI process and device characteristics, to make optimal trade-off between Area, Performance and Power.**
* **Good knowledge of standard cell libraries – circuit design and standard cell layout.**
* **Good Hands on Static timing analysis (STA), EM, IR, RV and sign-off flows.**
* **Good hands on experience of DFT methodologies.**
* **Prior experience with 16 nm and below technologies is plus.**
* **Must have experience in ECO flows for timing and layout cleanup.**
* **Need to help the convergence of integration of blocks at the top level.**
* **Develop, support and maintain physical design flows and methodologies.**
* **Work closely with the cross site design team to accomplish the project goals.**
* **Mentor the junior employees in terms of flows and design convergence.**
* **Worked on at least 6 tapeins of moderate to high speed designs with multiple voltages, clock domains and multi VT libraries.**
* **Self-driven individual and an excellent team player experienced in working with remote teams.**
* **Must have good communication skills and the ability and desire to work as a team.**

**Strong hands-on experience in following:**

* **Low power design techniques.**
* **Synthesis, Floor planning, place & route.**
* **Power optimization and clock tree distribution, pin placement and timing constraints generation.**
* **Hands on experience with UPF and multi PVT designs.**
* **Timing convergence using high speed design techniques with signal integrity ,Noise, EM, IR and RV.**
* **Physical design verification flows of DRC, LVS.**
* **Functional verification at various levels of design hierarchy with respect to golden RTL by formal methods.**
* **Good at scripting skills like perl, python, tcl.**

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